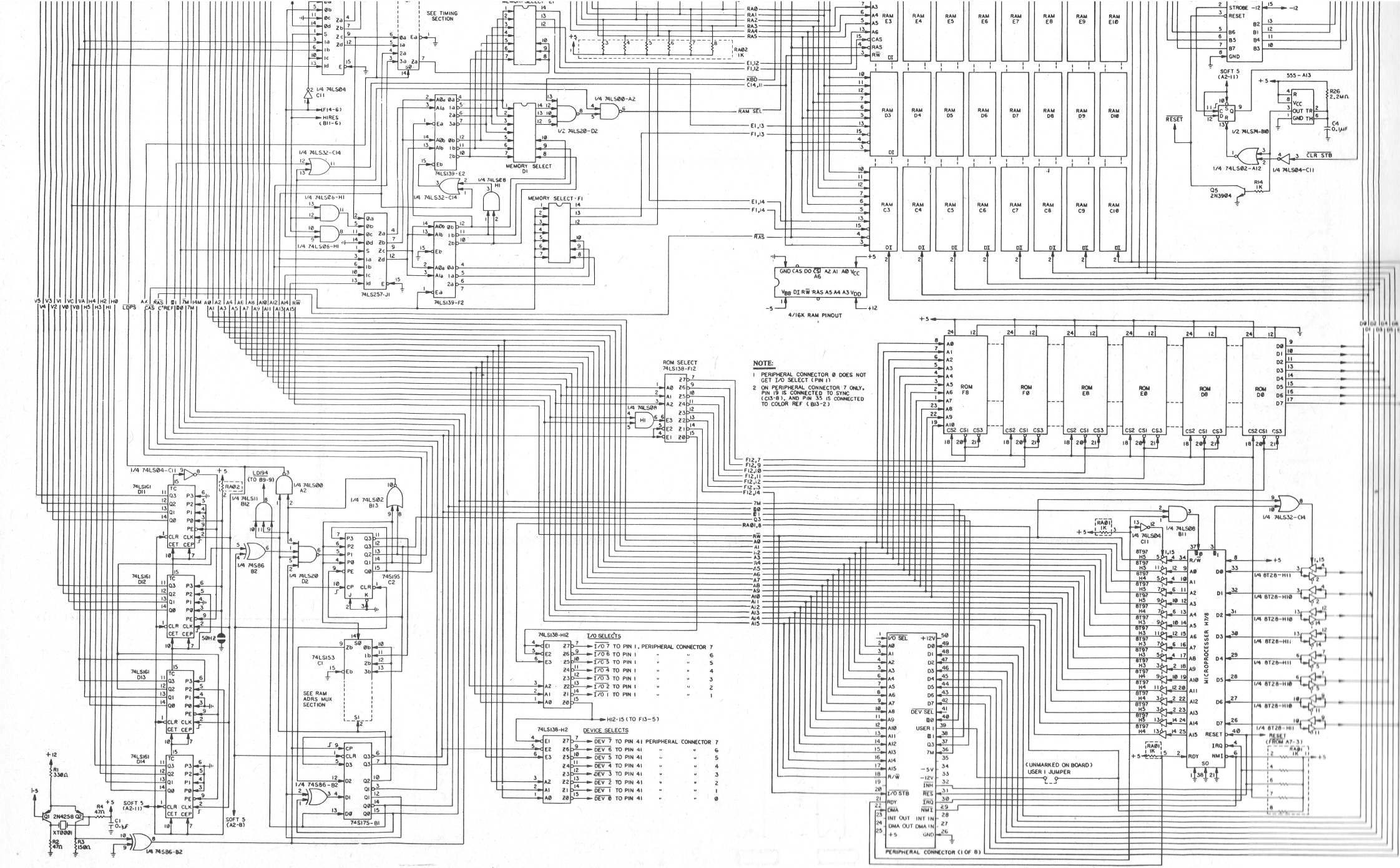
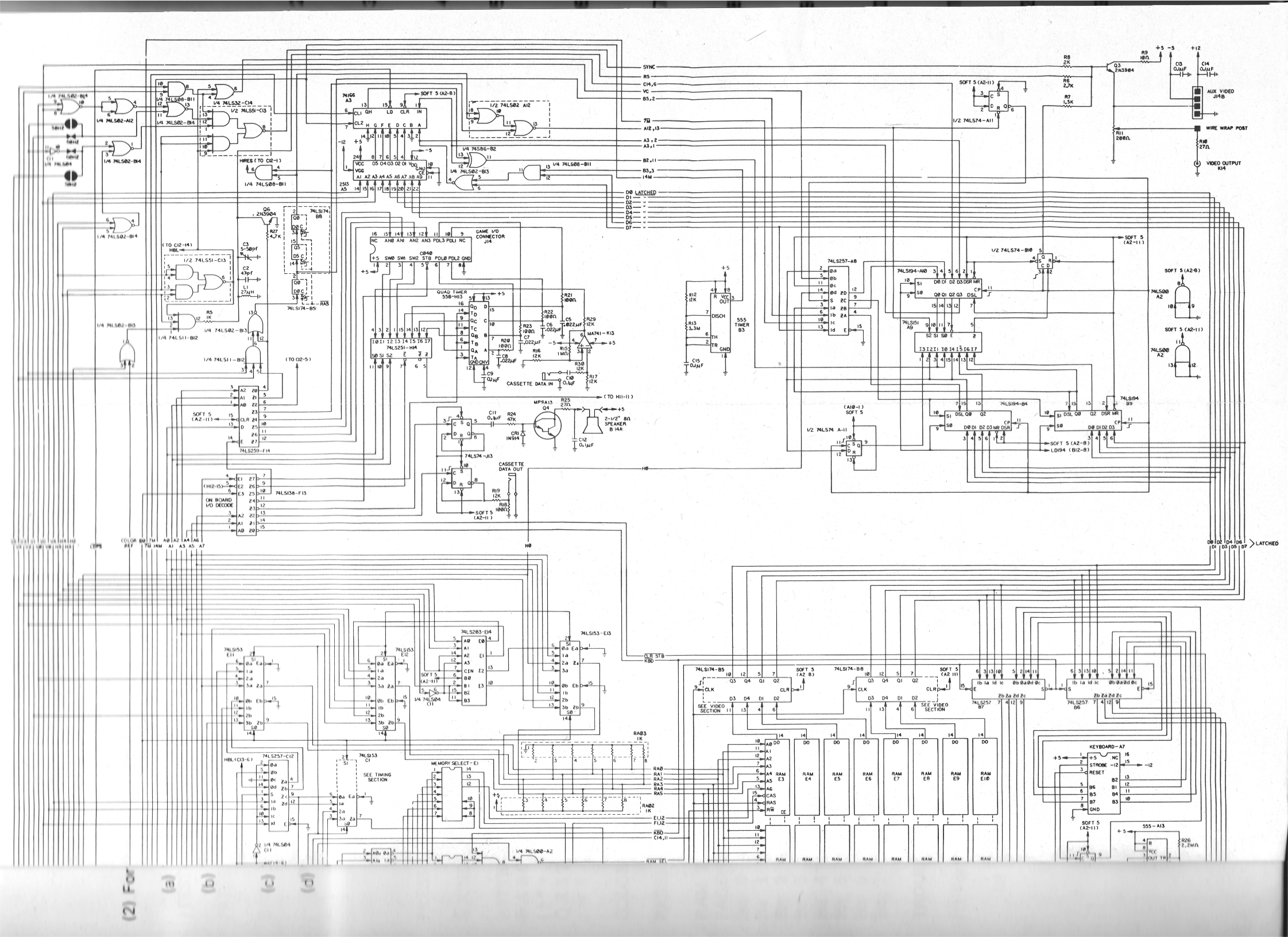
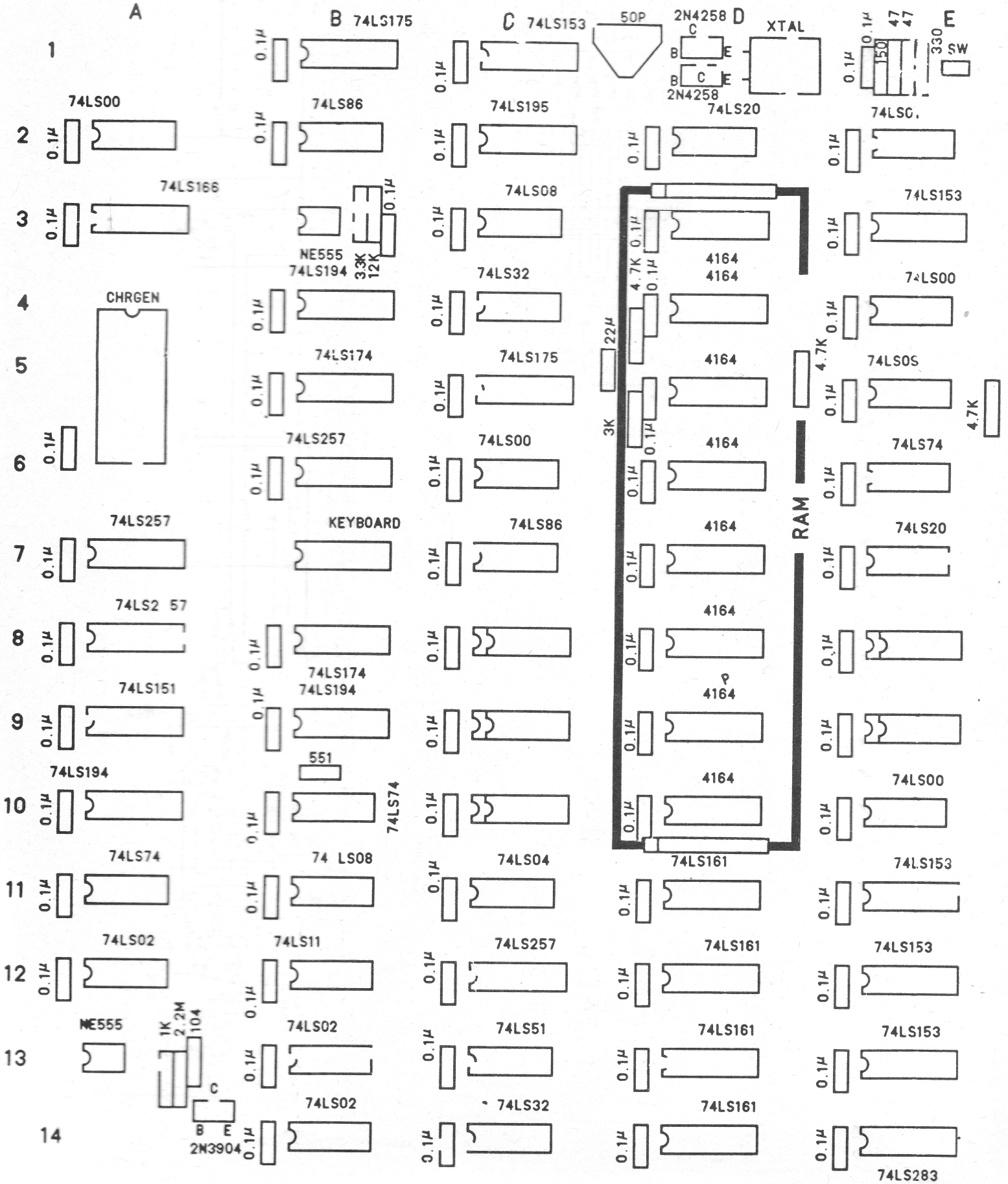

NOTE:
1 PERIPHERAL CONNECTOR 0 DOES NOT GET I/O SELECT (PIN 1)
2 ON PERIPHERAL CONNECTOR 7 ONLY, PIN 19 IS CONNECTED TO SYNC (C13-8), AND PIN 35 IS CONNECTED TO COLOR REF (B13-2)
4/16K RAM PINOUT
MEMORY SELECT
SEE TIMING SECTION
SEE RAM ADRS MUX SECTION
I/O SELECTS
DEVICE SELECTS
(UNMARKED ON BOARD) USER 1 JUMPER
PERIPHERAL CONNECTOR (1 OF 8)
MICROPROCESSER H7/8
ROM SELECT 74LS138-F12

BASE 48 CKT Diagram

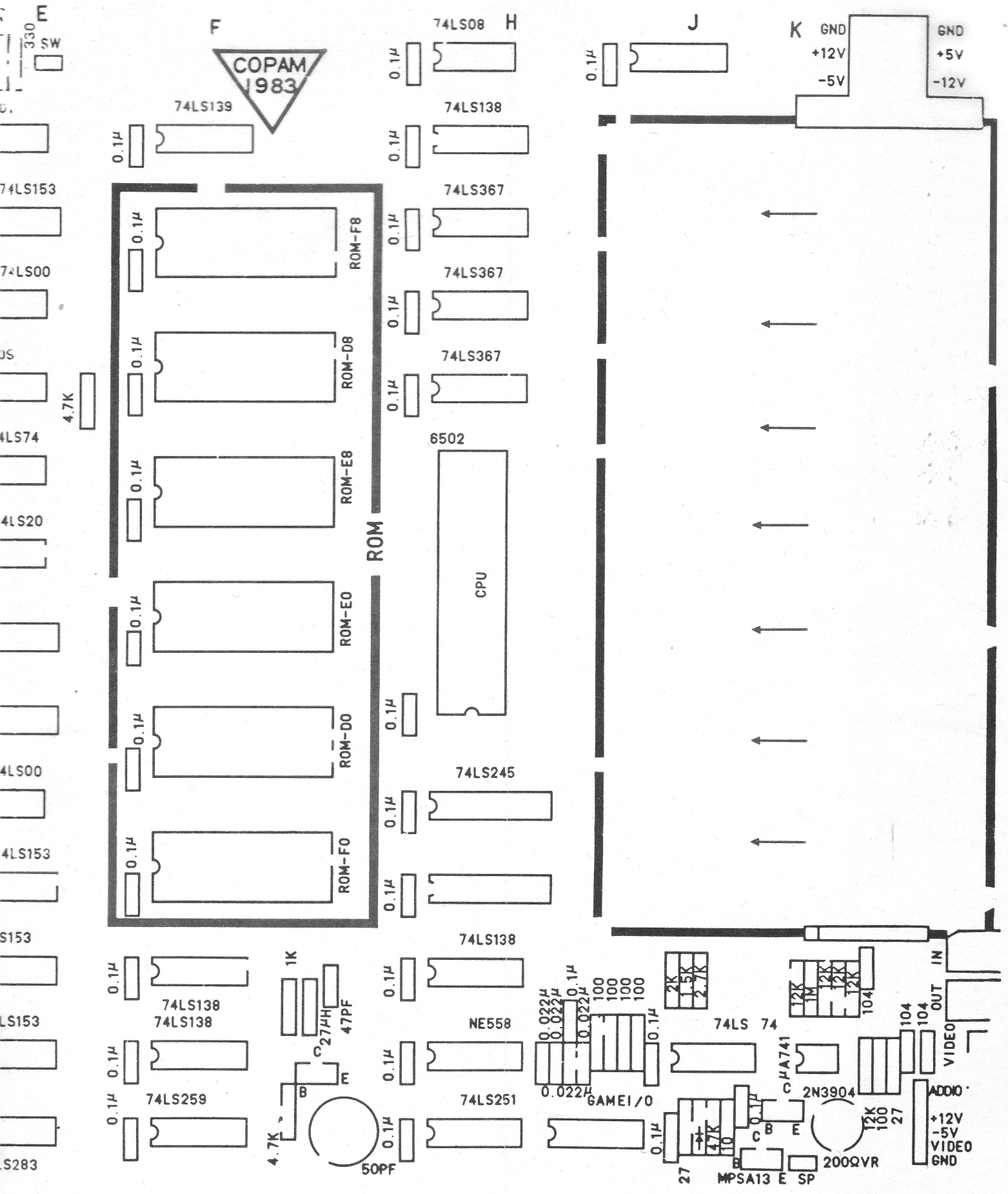

SYNC
R5
C14,6
VC
B5,2
7M
A12,13
A3,2
A3,1
B2,11
B3,3
14M
D0 LATCHED
D1
D2
D3
D4
D5
D6
D7
SOFT 5 (A2-B)
SOFT 5 (A2-11)
HIRES (TO C12-1)
(TO C12-14)
HBL
(TO C12-5)
RAS
GAME I/O CONNECTOR J14
QUAD TIMER 558-H13
CASSETTE DATA IN
CASSETTE DATA OUT
555 TIMER B3
MPSA13 Q4
2-1/2" 8Ω SPEAKER B 14A
AUX VIDEO J14B
WIRE WRAP POST
VIDEO OUTPUT K14
(TO H11-11)
H0
ON BOARD I/O DECODE
COLOR REF
CLR STB KBD
LATCHED
SEE VIDEO SECTION
SEE TIMING SECTION
MEMORY SELECT-E1
KEYBOARD-A7
555-A13
RAM E3
RAM E4
RAM E5
RAM E6
RAM E7
RAM E8
RAM E9
RAM E10

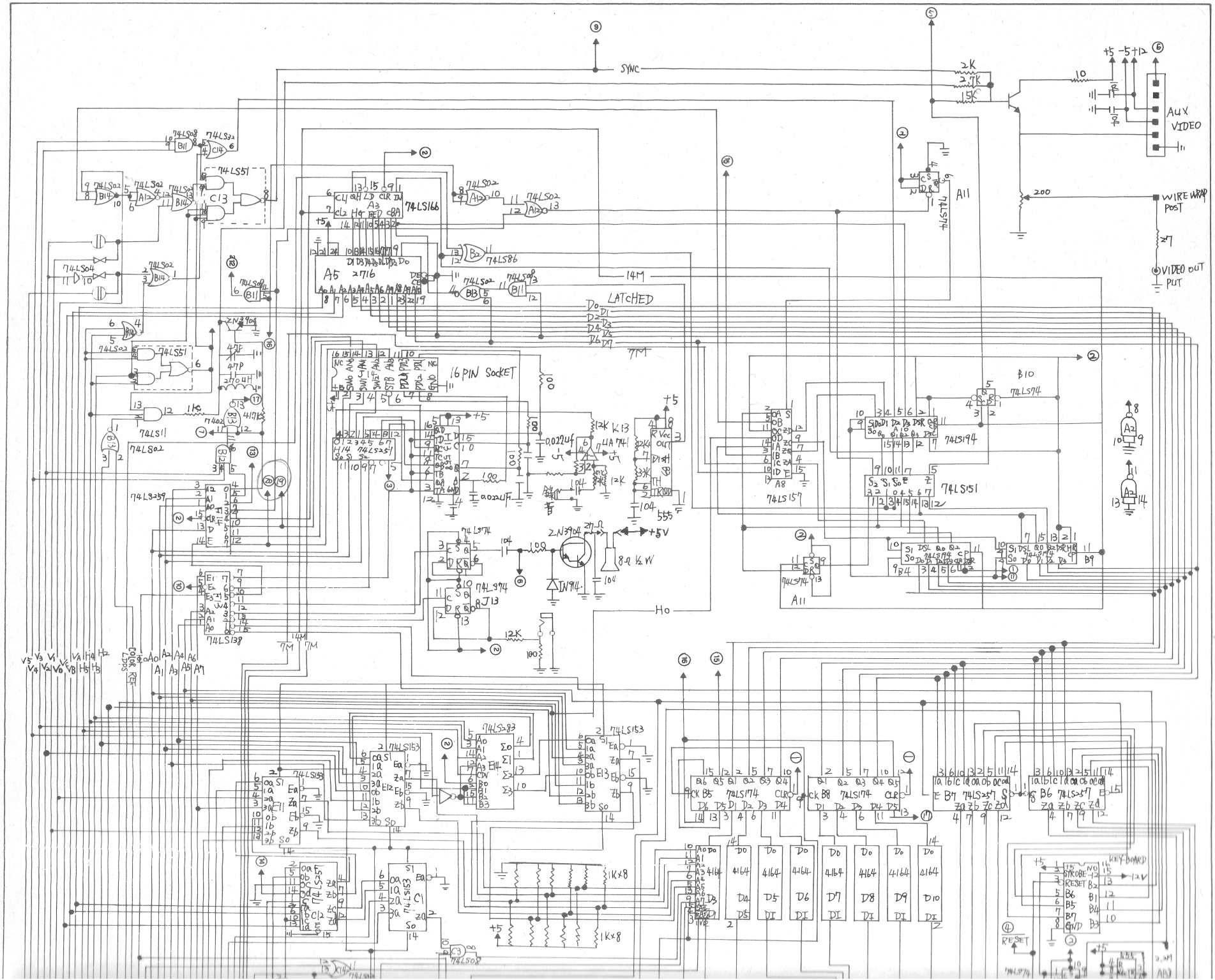
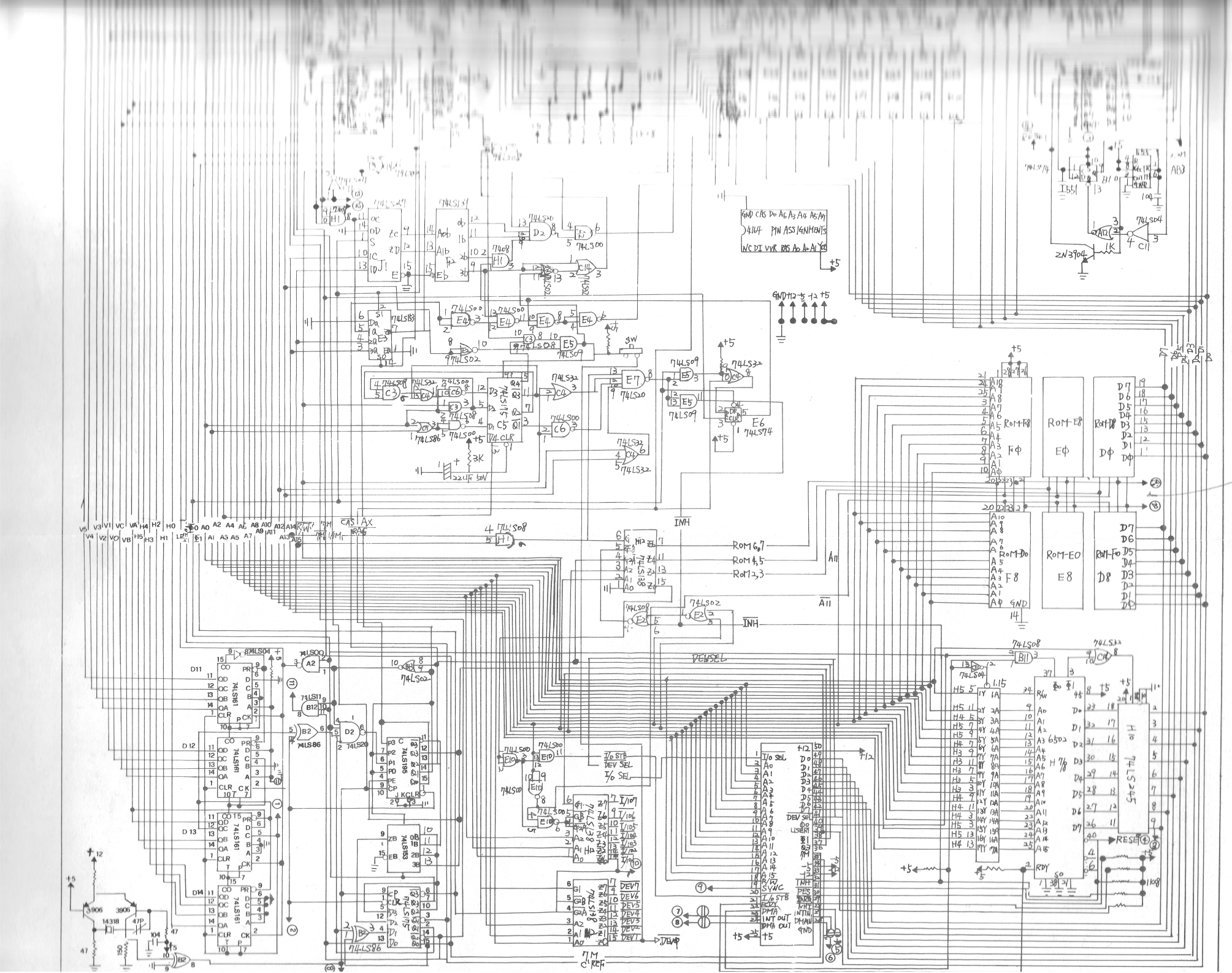
(2) For

BASE 64A Component



onent Location Diagram




SYNC
AUX VIDEO
WIRE WRAP POST
VIDEO OUT PUT
LATCHED
16 PIN SOCKET
74LS166
74LS174
74LS194
74LS157
74LS151
74LS374
74LS138
74LS153
74LS283
74LS257
74LS374
74LS374
74LS374

C4A CKT Diagram